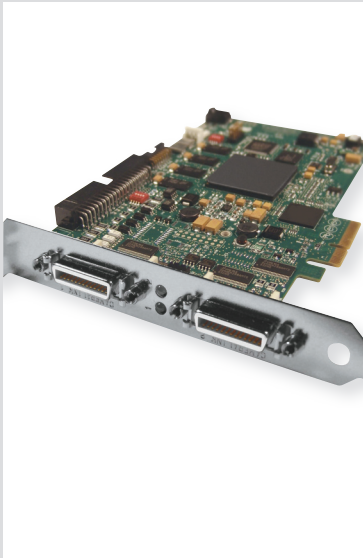


## X64 Xcelera-CL PX4 Dual PCI Express x4 Frame Grabbers



- Half-length PCI Express x4 Board
- Simultaneous acquisition from two Camera Link Base cameras
- Simultaneous acquisition from area and line scan monochrome and RGB digital cameras
- Rapid image acquisition rates up to 255MB/s per input channel
- Image transfer to host memory at 1024MB/s
- On-board FPGA based real-time Bayer decoding and shading correction of each input
- Power Over CameraLink Compliant (PoCL)
- Teledyne DALSA Platform Development Advantage – Free Run-time Licensing<sup>1</sup>



TRIGGER-TO-IMAGE  
RELIABILITY

## Fast, flexible, highly reliable image acquisition

Building on the field proven technology and performance of Teledyne DALSA's X64 frame grabbers the new X64 Xcelera Series leverages the PCI Express (PCIe) platform to bring traditional image acquisition and processing technology to new levels of performance and flexibility.

The PCIe host interface is a point to point host interface allowing simultaneous image acquisition and transfer without loading the system bus and involving little intervention from the host CPU. Designed with the requirements of the machine vision OEMs in mind, the Xcelera Series will range from entry level frame grabbers, to high-performance image acquisition boards, to embedded vision processors.

Addressing the emerging needs of bandwidth-hungry machine vision applications, Teledyne DALSA's Xcelera Series is defining next generation frame grabber capabilities with the ability to deliver bandwidth of 1GB/sec over multiple-lane PCI Express implementations with room to grow.

The X64 Xcelera-CL PX4 Dual is a highly versatile PCIe frame grabber capable of acquiring images from two independent Camera Link™ Base cameras and performing image transfers at rates up to 1024MB/s. Its low cost, combined with its ability to support multiple tap configurations from area and line scan monochrome/RGB cameras simultaneously; in addition to its on-board FPGA Bayer decoding and real-time shading correction makes the X64 Xcelera-CL PX4 Dual an ideal solution to a wide variety cost-sensitive applications.

The X64 Xcelera-CL PX4 Dual has been built within Teledyne DALSA's Trigger-to-Image Reliability technology framework. Trigger-to-Image Reliability leverages Teledyne DALSA's hardware and software innovations to control, monitor and correct the image acquisition process from the time that an external trigger event occurs to the moment the data is sent to the host, providing traceability when errors do occur and permitting recovery from those errors.

### Software Support

All of the frame grabbers in the Xcelera series are supported by Teledyne DALSA's Sopera Essential software package. Sopera Essential, is a cost-effective machine vision software toolkit that bundles board level acquisition and control with advanced image processing capability, featuring a value added, all new geometric search tool.

Sopera Essential is designed to deliver the critical functionality needed to design, develop and deploy high-performance machine vision applications while at the same time significantly lowering deployment costs.

### Teledyne DALSA Platform Development Advantage - Free Run-Time Licensing

The Sopera Essential standard processing tool run-time license is offered at no additional charge when combined with the Teledyne DALSA frame grabbers. This software run-time license<sup>1</sup> includes access to over 400 image processing functions, area-based (normalized correlation based) template matching tool, blob analysis and lens correction tool.

<sup>1</sup> Some conditions and limitations apply, contact Teledyne DALSA sales for details.

# X64 Xcelera-CL PX4 Dual

## PCI Express x4 Frame Grabbers

### Specifications

| Function                                  | Description  | Function                         | Description   |
|---|--|----------------------------------|---|
| <b>Board</b>                              | Camera Link Specifications Rev 1.10 compliant<br>Half length PCI Express 1.0a x4 compliant<br>ROHS Compliant   | <b>Controls</b>                  | Comprehensive event notification includes end/start-of-field/frame/transfer<br>Independent timing control logic for up to two Camera Link cameras<br>Two optically isolated TTL/LVDS trigger inputs programmable as active high or low (edge or level trigger)<br>Two independent TTL Strobes outputs<br>Two PC independent serial communications ports provide support 9600 to 11500K baud<br>Appear as system serial ports enabling seamless interface to host applications<br>Optically isolated quadrature (AB) shaft-encoder inputs for external web synchronization<br>Supports up/down scaling |
| <b>Acquisition</b>                        | Supports two independent Base or one Medium Camera Link area and line scan cameras<br>Acquisition pixel clock rates up to 85MHz  | <b>On-board I/Os<sup>2</sup></b> | 4-optically general purpose inputs tolerate 5V and 24V DC signals 4 general purpose outputs<br>PoCL compliant (4W max.)<br>Power-on-reset fused +12V output @ 1.5A<br>+5V DC output at 1.5A   |
| <b>Resolution</b>                         | Horizontal Size (min/max): 8 byte/256K bytes<br>Vertical Size (min/max):<br>1 line/infinite lines for line-scan cameras<br>1 line/16million lines/frame for area-scan cameras<br>Variable length frame size from 1 to 16 million lines for area-scan cameras<br>128MB onboard frame buffer memory<br>Integrated advanced tap reversal engine allows independent tap formatting | <b>Power Output</b>              | Device driver supports:<br>Microsoft Windows, XP and Vista compliant<br>Supports Microsoft Windows Vista and XP Professional 64-bit <sup>3</sup><br>Full support of Teledyne DALSA's Sapera Essential, Sapera LT and Sapera Processing software libraries<br>Application development using C++ DLLs and ActiveX controls with Microsoft Visual Studio version 6.0 or higher   |
| <b>Pixel Format and Tap configuration</b> | Supports Camera Link tap configurations for 8, 10, or 12-bit mono, and RGB:<br>For Base cameras in any of the following combinations:<br>3x8-bit/tap, 2x10-bits/tap, 2x12-bit/tap, 1x14-bit/tap, 1x16-bits/tap, & 1x24-bit/RGB<br>For Medium camera - 4x8-bit/tap, 4x10-bits/tap, 4x12-bit/tap, 1x30-bit/RGB, & 1x36-bits/tap  | <b>Software</b>                  | PCI Express 1.0a compliant with one x4 slot system with 64MB or higher system memory<br>6.375" (16.1cm) Length X 4.20" (10.7 cm) Height<br>0°C (32° F) to 55° C (131° F)<br>Relative Humidity: up to 95% (non-condensing)<br>FCC Class B—Approved<br>CE—Approved  |
| <b>Transfers</b>                          | Real-time transfers to system memory<br>Intelligent Data-Transfer-Engine automatically loads scatter-gather and tap description tables from the host memory without CPU intervention   | <b>System Requirements</b>       |   |
| <b>On-board Processing</b>                |  | <b>Dimensions</b>                |   |
| Bayer Mosaic Filter                       | Hardware Bayer Engine supports one 8 and 10 bit Bayer camera input<br>Bayer output format supports 8 or 10-bit RGB/pixel<br>Zero host CPU utilization for Bayer conversion   | <b>Temperature</b>               |   |
| Shading Correction                        | On the fly Flat-line and Flat-field correction with dead-pixel replacement<br>Supports two independent monochrome cameras concurrently<br>User programmable calibration gain/offset maps   | <b>Markings</b>                  |   |
| Lookup Tables                             |  |                                  |   |
| <i>Monochrome</i>                         | Each input port has one 256x8-bit, 1024x10-bit, 1024x8-bit, 4096x12-bit, 4096x10-bit or 4096x8-bit OLLUTs  |                                  |   |
| <i>Colour</i>                             | Each input port has one 8-bit in/out, 10-bit in 8 or 10-bit out, 12-bit in 10 or 8-bit/out Lookup table  |                                  |   |

<sup>2</sup> Requires a separate slot for the bracket assembly

<sup>3</sup> Contact Teledyne DALSA Sales for more details

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