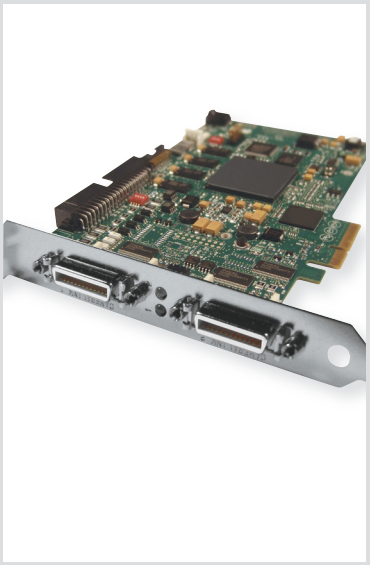
X64 Xcelera-CL PX4 Full

PCI Express x4 Frame Grabbers



Key Features

- Half-length PCI Express x4 Board
- Acquires images from one Base, Medium or Full Camera Link® camera
- Rapid image acquisition rates up to 1GB/s and high-speed image transfer to host memory at 1GB/s
- Supports Camera Link operations up to 85MHz
- Extended feature set supports non-Camera Link pixel/tap configurations
- Windows Vista and XP Professional (32/64-bit) compatible
- ROHS compliant
- On-board FPGA based real-time Bayer decoding and shading correction of each input
- Power Over CameraLink (PoCL) Compliant
- Teledyne DALSA Platform Development Advantage – Free Run-time Licensing[1]

TRIGGER-TO-IMAGE RELIABILITY

Advanced PCIe x4 image acquisition

Building on the field proven technology and performance of Teledyne DALSA's X64 frame grabbers the new X64 Xcelera Series leverages the PCI Express (PCIe) platform to bring traditional image acquisition and processing technology to new levels of performance and flexibility.

The PCIe host interface is a point-to-point host interface allowing simultaneous image acquisition and transfer without loading the system bus and involving little intervention from the host CPU. Designed with the requirements of the machine vision OEMs in mind, the Xcelera Series will range from entry level frame grabbers, to high-performance image acquisition boards, to embedded vision processors.

Addressing the emerging needs of bandwidth-hungry machine vision applications, Teledyne DALSA's Xcelera Series is defining next generation frame grabber capabilities with the ability to deliver bandwidth of 1GB/sec over multiple-lane PCI Express implementations with room to grow.

The X64 Xcelera-CL PX4 Full is a Camera Link frame grabber that is based on the PCI Express x4 interface. Compatible with a Base, Medium or Full Camera Link® camera, the X64 Xcelera-CL PX4 Full supports a wide variety of multi-tap area and line scan colour and monochrome cameras. For greater versatility, the X64 Xcelera-CL PX4 Full board can interface with camera pixel depths and tap configurations not covered by the Camera Link standard. For example, the Xcelera-CL PX4 Full can support 10-taps or higher with 8-bits per tap.

The X64 Xcelera-CL PX4 Full has been built within Teledyne DALSA's Trigger-to-Image Reliability technology framework. Trigger-to-Image Reliability leverages Teledyne DALSA's hardware and software innovations to control, monitor and correct the image acquisition process from the time that an external trigger event occurs to the moment the data is sent to the host, providing traceability when errors do occur and permitting recovery from those errors.

Software Support

All of the frame grabbers in the Xcelera series are supported by Teledyne DALSA's Sapera Essential software package. Sapera Essential, is a cost-effective machine vision software toolkit that bundles board level acquisition and control with advanced image processing capability, featuring a value added, all new geometric search tool.

Sapera Essential is designed to deliver the critical functionality needed to design, develop and deploy high-performance machine vision applications while at the same time significantly lowering deployment costs.

Teledyne DALSA Platform Development Advantage - Free Run-Time Licensing

The Sapera Essential standard processing tool run-time license is offered at no additional charge when combined with the Teledyne DALSA frame grabbers. This software run-time license[1] includes access to over 400 image processing functions, area-based (normalized correlation based) template matching tool, blob analysis and lens correction tool.

[1] Some conditions and limitations apply, contact Teledyne DALSA sales for details.

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X64 Xcelera-CL PX4 Full

PCI Express x4 Frame Grabbers

Specifications

Function	Description
Board	Camera Link Specifications Rev 1.10 compliant
	Half length PCI Express 1.0a x4 compliant
	ROHS Compliant
Acquisition	Supports one Base, Medium or Full Camera Link area and line scan camera
	Acquisition pixel clock rates up to 85MHz
Resolution	Horizontal Size (min/max): 8 byte/256K bytes
	Vertical Size (min/max): 1 line/infinite lines for line-scan cameras 1 line/16million lines/frame for area-scan cameras
	Variable length frame size from 1 to 16 million lines for area-scan cameras
	128MB onboard frame buffer memory
	Integrated advanced tap reversal engine allows independent tap formatting
Pixel Format and Tap configuration	Supports Camera Link tap configurations for 8, 10, or 12-bit mono, and RGB:
	For Base cameras in any of the following combinations: 3x8-bit/tap, 2x10-bits/tap, 2x12-bit/tap, 1x14-bit/tap, 1x16-bits/tap, & 1x24-bit/RGB
	For Medium camera - 4x8-bit/tap, 4x10-bits/tap, 4x12-bit/tap, 1x30-bit/RGB, & 1x36-bits/tap
	For Full—8x 8-bit/tap Camera Link ; 10x8-bit non-Camera Link configuration
Transfers	Real-time transfers to system memory
	Intelligent Data-Transfer-Engine automatically loads scatter-gather and tap description tables from the host memory without CPU intervention
On-board Processing	
Bayer Mosaic Filter	Hardware Bayer Engine supports one CameraLink Base 8, 10 or 12-bit Bayer
	Bayer output format supports 8 or 10-bit RGB/pixel
	Zero host CPU utilization for Bayer conversion
Shading Correction	On the fly Flat-line and Flat-field correction with dead-pixel replacement
	Supports Camera Link Base, Medium or Full cameras
	User programmable calibration gain/offset maps
Output Lookup Tables	
Monochrome	Each input port has one 256x8-bit, 1024x10-bit, 1024x8-bit, 4096x12-bit, 4096x10-bit or 4096x8-bit OLUTs
Colour	Each input port has one 8-bit in/out, 10-bit in 8 or 10-bit out, 12-bit in 12, 10 or 8-bit/out Lookup table

Function	Description
Controls	Comprehensive event notification includes end/start-of-field/frame/transfer
	Camera control signals for external event synchronization
	Optically isolated TTL/LVDS trigger inputs programmable as active high or low (edge or level trigger)
	TTL Strobes outputs
	PC independent serial communications ports provide support 9600 to 11500K baud Appear as system serial ports enabling seamless interface to host applications
Shaft-Encoder Input	Optically isolated quadrature (AB) shaft-encoder inputs for external web synchronization Supports up/down scaling
On-board I/Os[2]	4-optically general purpose inputs tolerate 5V and 24V DC signals 4 general purpose outputs
Power Output	PoCL Compliant (4W max) Power-on-reset fused +12V output @ 1.5A +5V DC output at 1.5A
Software	Device driver supports: Microsoft Windows XP and Vista compliant Supports Microsoft Windows Vista and XP Professional 64-bit[3]
	Full support of Teledyne DALSA DIGITAL IMAGING's Sapera Essential, Sapera LT and Sapera Processing software libraries
	Application development using C++ DLLs and ActiveX controls with Microsoft Visual Studio
System Requirements	PCI Express 1.0a compliant with one x4 slot system with 64MB or higher system memory
Dimensions	6.375" (16.1cm) Length X 4.20" (10.7 cm) Height
Temperature	0°C (32° F) to 55° C (131° F)
	Relative Humidity: up to 95% (non-condensing)
Markings	FCC Class B—Approved
	CE—Approved

[2] Requires a separate slot for the bracket assembly
[3] Contact Teledyne DALSA sales for more details.

www.teledynedalsa.com

Americas
Boston, USA
Tel: +1 978-670-2000
sales.americas@teledynedalsa.com

Europe
Munich, Germany
Tel: +49 8142-46770
sales.europe@teledynedalsa.com

Asia Pacific
Tokyo, Japan
+81 3-5960-6353
sales.asia@teledynedalsa.com

Teledyne DALSA is an international leader in digital imaging and semiconductors and has its corporate offices in Waterloo, Ontario, Canada.

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